CLAIMS

What is claimed is:

1. An integrated circuit device comprising:

   a) a plurality of signal lines disposed within a substrate;

   b) a power grid disposed on said substrate and comprising: a plurality of power lines having a first thickness; and a plurality of ground lines having said first thickness, said power grid for supplying power and ground to circuitry of said substrate; and

   c) a shield mesh disposed on said substrate and comprising of a plurality of power lines having a second thickness; and a plurality of ground lines having said second thickness, wherein respective signal lines of said plurality of signal lines are disposed between a respective power line of said shield mesh and a respective ground line of said shield mesh, said shield mesh for reducing the effects of electronic cross-talk between nearby signal lines of said plurality of signal lines.

2. An integrated circuit as described in Claim 1 wherein said second thickness is less than said first thickness.

3. An integrated circuit as described in Claim 2 wherein said signal lines of said plurality of signal lines are as thick as said second thickness.

4. An integrated circuit as described in Claim 1 wherein said power and ground lines of said shield mesh are alternatively disposed and parallel to each other within a single metal layer of said substrate.

5. An integrated circuit as described in Claim 3 wherein said power and ground lines of said shield mesh are aligned with substrate grid lines.

6. An integrated circuit as described in Claim 1 wherein said power and ground lines of said shield mesh are alternatively disposed in a first direction parallel to each other within a first metal layer of said substrate and wherein said power and ground lines of said shield mesh are also alternatively disposed in a second direction parallel to each other within a second metal layer of said substrate, said second metal layer being underneath said first metal layer and wherein said first and second directions are 90 degrees apart.

7. An integrated circuit as described in Claim 1 wherein said electronic cross-talk comprises capacitive and inductive coupling.

8. An integrated circuit device comprising:

a) a plurality of signal lines disposed within a substrate;

b) a power grid disposed on said substrate and comprising: a plurality of first lines having a first thickness and for supplying a first voltage level; and a plurality of second lines having said first

thickness and for supplying a second voltage level, said power grid for supplying power to circuitry of said substrate;

c) a shield mesh disposed on said substrate and comprising: a plurality of third lines having a second thickness and for supplying said first voltage level; and a plurality of fourth lines having said second thickness and for supplying said second voltage level, wherein respective signal lines of said plurality of signal lines are disposed between a respective third line of said shield mesh and a respective fourth line of said shield mesh, said shield mesh for reducing the effects of electronic cross-talk between nearby signal lines of said plurality of signal lines.

9. An integrated circuit as described in Claim 8 wherein said second thickness is less than said first thickness.

10. An integrated circuit as described in Claim 9 wherein said signal lines of said plurality of signal lines are as thick as said second thickness.

11. An integrated circuit as described in Claim 8 wherein said third and fourth lines of said shield mesh are alternatively disposed and parallel to each other within a single metal layer of said substrate.

12. An integrated circuit as described in Claim 10 wherein said third and fourth lines of said shield mesh are aligned with substrate grid lines.

13. An integrated circuit as described in Claim 8 wherein said third and fourth lines of said shield mesh are alternatively disposed in a first direction parallel to each other within a first metal layer of said substrate and wherein said third and fourth lines of said shield mesh are also alternatively disposed in a second direction parallel to each other within a second metal layer of said substrate, said second metal layer being underneath said first metal layer and wherein said first and second directions are 90 degrees apart.

14. An integrated circuit as described in Claim 13 wherein third lines of said first metal layer and third lines of said second metal layer are coupled together using first connections.

15. An integrated circuit as described in Claim 14 wherein fourth lines of said first metal layer and fourth lines of said second metal layer are coupled together using second connections.

16. An integrated circuit as described in Claim 8 wherein said electronic cross-talk comprises capacitive and inductive coupling.

17. An integrated circuit as described in Claim 8 wherein said shield mesh consumes substantially 50 percent of the available area of said substrate.

18. An integrated circuit device comprising:

a) a plurality of signal lines disposed within a substrate;

b) a power grid disposed on said substrate and comprising plurality of power lines having a first thickness; and a plurality of ground lines having said first thickness, said power grid for supplying power and ground to circuitry of said substrate; and

c) a shield mesh disposed on said substrate and comprising plurality of first lines having a second thickness; and a plurality of second lines having said second thickness, wherein respective signal lines of said plurality of signal lines are disposed between a respective first line of said shield mesh and a respective second line of said shield mesh, said shield mesh for reducing the effects of electronic cross-talk between nearby signal lines of said plurality of signal lines.

19. An integrated circuit as described in Claim 18 wherein said first and second lines of said shield mesh are alternatively disposed and parallel to each other within a single metal layer of said substrate.

20. An integrated circuit as described in Claim 18 wherein said first and second lines of said shield mesh are alternatively disposed in a first direction parallel to each other within a first metal layer of said substrate and wherein said first and second lines of said shield mesh are also alternatively disposed in a second direction parallel to each other within a second metal layer of said

substrate, said second metal layer being underneath said first metal layer and wherein said first and second directions are 90 degrees apart.